

**JF J****5 I H 8 F**

- A package consists of four dual anti-parallel SCR chips
- Welding by vacuum welding technology, which provide high reliability
- Insulated by silicone gel, provide a insulation voltage of 3000V~

& HF

- Soft start
- Solid state relay
- AC/DC switch
- Temperature control

&G J 2 F F L (@ T_C = 25 °C unless otherwise specified)

5F F J J	(I	8 G	F J	
Repetitive peak off-state voltage	Tvj = 25 °C	V _{DRM}	1800	V
Repetitive peak reverse voltage	Tvj = 25 °C	V _{RRM}	1800	V
Non-repetitive peak off-state voltage	Tvj = 25 °C	V _{DSM}	1900	V
Non-repetitive peak reverse voltage	Tvj = 25 °C	V _{RSM}	1900	V
RMS on-state current	T _C = 80 °C	I _{T(RMS)}	50	A
Forward surge current	1/2 cycle, Sine wave, 50Hz Tvj = 25°C	I _{TSM}	500	A
I ² t value for fusing		I ² t	1250	A ² s
Critical rate of rise of on-state current	I _G =2×I _{GT}	di/dt	150	A/μs
RMS isolation voltage	A.C 50Hz(1s/1min)	V _{ISO}	3000/2500	V
Junction temperature range		T _J	-40 ~ +125	°C
Storage temperature range		T _{stg}	-40 ~ +125	°C

JH HF (MF FH J H (@ T_C = 25 °C unless otherwise specified)

5F F J J	(I	8 G	F J			
			2		2F	
Peak forward voltage	$I_T=75A, t_p=380\mu s$	V_T			1.90	V
Repetitive peak off-state current	$V_D = V_{DRM}, T_{vj} = 25^\circ C$	I_{DRM}			500	μA
	$V_D = V_{DRM}, T_{vj} = 125^\circ C$				10	mA
Reverse leakage current	$V_R = V_{RRM}, T_{vj} = 25^\circ C$	I_{RRM}			500	μA
	$V_R = V_{RRM}, T_{vj} = 125^\circ C$				10	mA
Threshold voltage	For power loss calculation only $T_{vj} = 125^\circ C$,	V_{TO}			1.0	V
Dynamic resistance	$T_{vj} = 125^\circ C$,	r_T			8	m Ω
Triggering gate current	$V_D=12V R_L=30\Omega$	I_{GT}	20		120	mA
Holding current	$I_T=1A$	I_H			150	mA
Latching current	$I_G=1.2 I_{GT}$	I_L			300	mA
Critical rate of rise of voltage	$V_D=2/3V_{DRM} T_{vj}=125^\circ C$ Gate Open	dv/dt	1000			V/ μs
Triggering gate voltage	$V_D=12V R_L=30\Omega$	V_{GT}			1.5	V
Non triggering gate voltage	$V_D=V_{DRM} T_{vj}=125^\circ C$	V_{GD}	0.2			V

MU F (MF FH J H (@ T_C = 25 °C unless otherwise specified)

5F F J J	(I	8 G	F J			
			2		2F	
Thermal resistance, junction to case	per Thyristor	$R_{th(j-c)}$		1.2		/W
Mounting torque	Module torque to heatsink	M	1.8		2.0	N m

I J L K F

) J HJ	2F L	5FH FLJ	J LM	. J	5J (F
JMT50WT18S2C	JMT50WT18S2C	S2	16.8g/PCS	90 PCS	810 PCS

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FIG.1: Forward characteristics(per thyristor)

FIG.2: Surge overload current vs. time

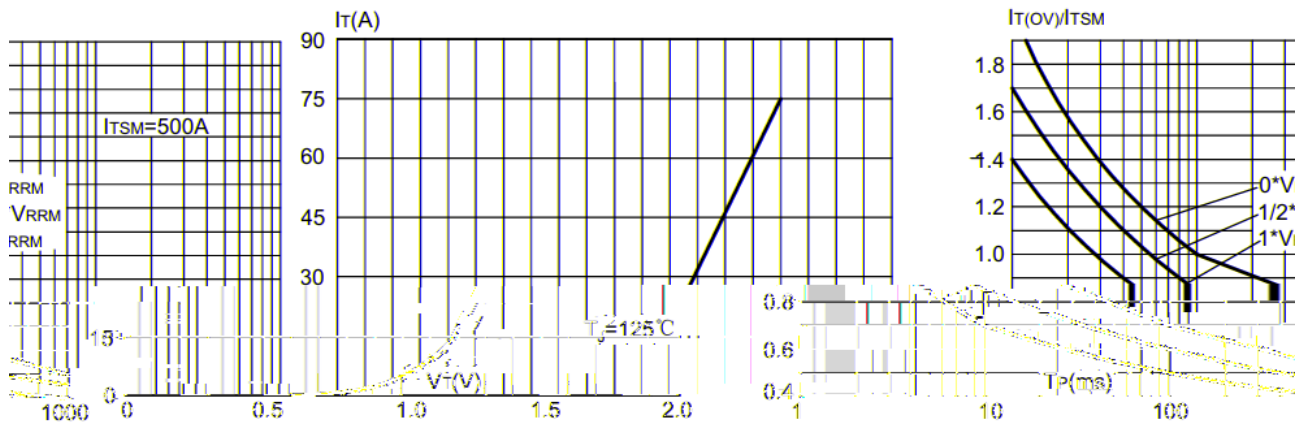
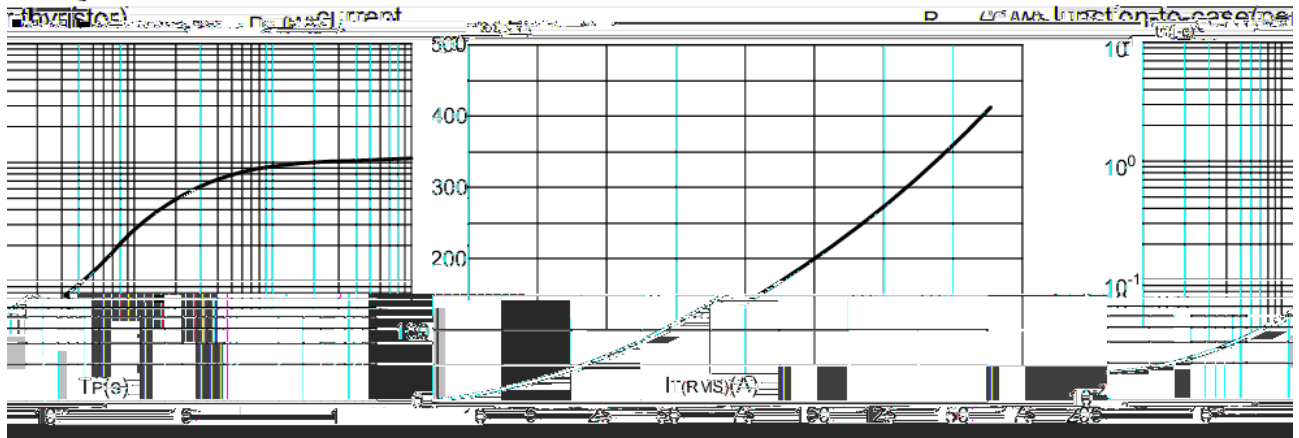
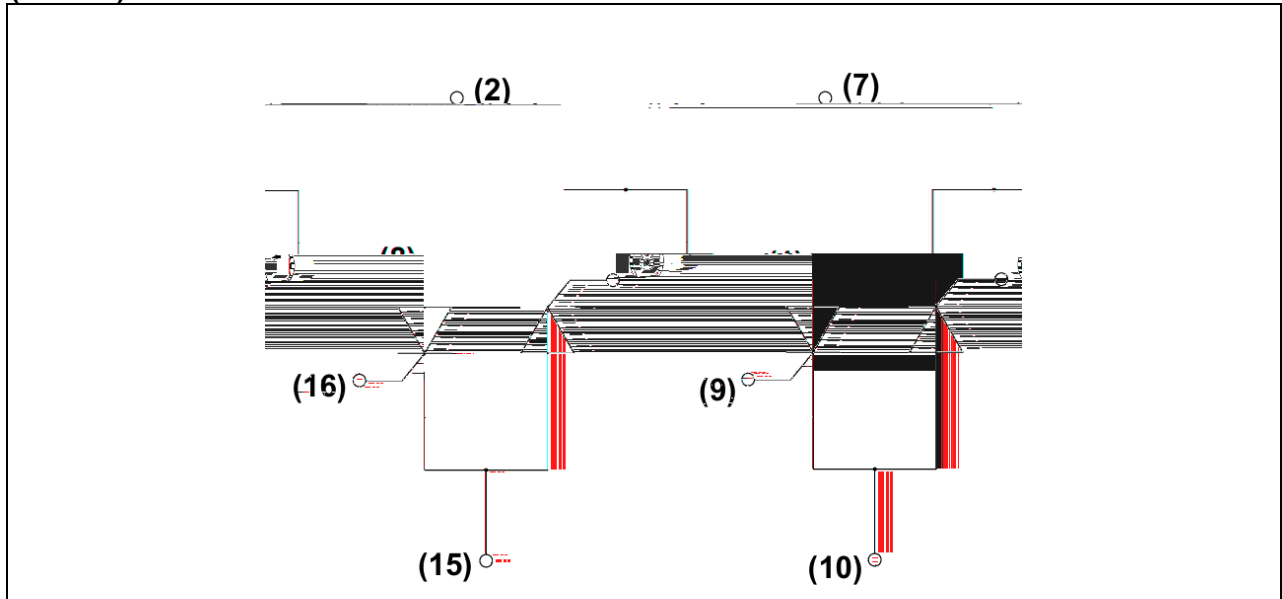


FIG.3: Power dissipation per module vs. R.M.S.

FIG.4: Maximum transient thermal impedance



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5FH FLJ J

